Vector Processor : Memory Banks

- The behavior of the load/store vector unit is significantly more complicated than that of the arithmetic functional units. The start-up time for a load is the time to get the first word from memory into a register. If the rest of the vector can be supplied without stalling, then the vector initiation rate is equal to the rate at which new words are fetched or stored. Unlike simpler functional units, the initiation rate may not necessarily be one clock cycle because memory bank stalls can reduce effective throughput.

- Typically, penalties for start-ups on load/store units are higher than those for arithmetic units-over 100 clock cycles on many processors. For VMIPS we assume a start-up time of 12 clock cycles.

- To maintain an initiation rate of one word fetched or stored per clock, the memory system must be capable of producing or accepting this much data. Spreading accesses across multiple independent memory banks usually delivers the desired rate.

- Most vector processors use memory banks, which allow multiple independent accesses rather than simple memory interleaving for three reasons:

  1. Many vector computers support multiple loads or stores per clock, and the memory bank cycle time is usually several times larger than the processor cycle time. To support simultaneous accesses from multiple loads or stores, the memory system needs multiple banks and to be able to control the addresses to the banks independently.

  2. Most vector processors support the ability to load or store data words that are not sequential. In such cases, independent bank addressing, rather than inter   leaving, is required.

  3. Most vector computers support multiple processors sharing the same memory system, so each processor will be generating its own independent stream of addresses.